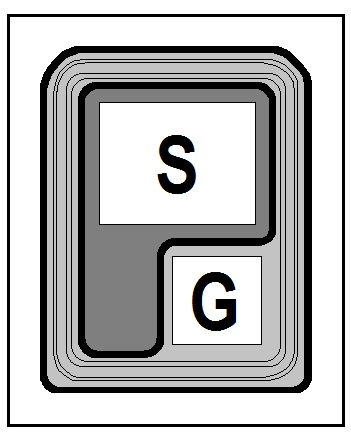
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.018”**

**.022”**

**Top Material: Al**

**Backside Material: Au**

**G = .0047” X .0047”**

**S = .0071” X .0079”**

**Backside Potential: Drain**

**APPROVED BY: DK DIE SIZE .018” X .022” DATE: 12/15/22**

**MFG: FAIRCHILD THICKNESS .005” P/N: 2N7000**

**DG 10.1.2**

#### Rev B, 7/19/02